# Laboratory Exercise 7

### Finite State Machines

This is an exercise in using finite state machines.

**Part I**

We wish to implement a finite state machine (FSM) that recognizes two specific sequences of applied input sym- bols, namely four consecutive 1s or four consecutive 0s. There is an input *w* and an output *z*. Whenever *w* = 1 or *w* = 0 for four consecutive clock pulses the value of *z* has to be 1; otherwise, *z* = 0. Overlapping sequences are allowed, so that if *w* = 1 for five consecutive clock pulses the output *z* will be equal to 1 after the fourth and fifth pulses. Figure [1](#_bookmark39) illustrates the required relationship between *w* and *z*.

Clock

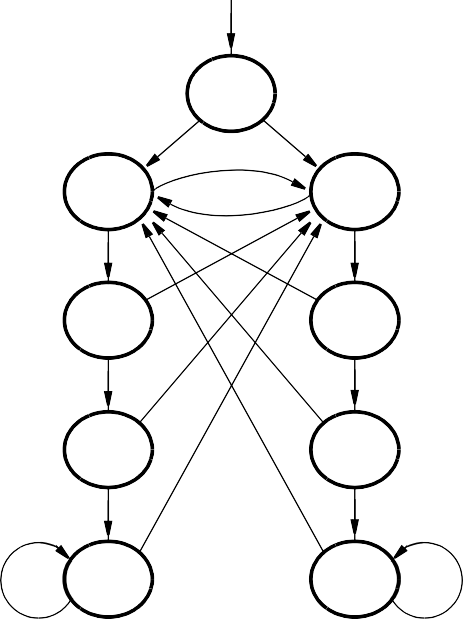
*w z*

Figure 1: Required timing for the output *z*.

A state diagram for this FSM is shown in Figure [2](#_bookmark40). For this part you are to manually derive an FSM circuit that implements this state diagram, including the logic expressions that feed each of the state flip-flops. To implement the FSM use nine state flip-flops called *y*8*, . . . , y*0 and the one-hot state assignment given in Table [1](#_bookmark41).

Reset

0 1



A/0

*w* = 0

*w* = 1

B/0

1

0

F/0

*w* = 0

1

1 0

C/0 G/0

*w* = 0

1

0

1

D/0

1

0

H/0

*w* = 0

1

E/1

I/1

Figure 2: A state diagram for the FSM.

|  |  |
| --- | --- |
| Name | State Code  *y*8*y*7*y*6*y*5*y*4*y*3*y*2*y*1*y*0 |
| **A** | 000000001 |
| **B** | 000000010 |
| **C** | 000000100 |
| **D** | 000001000 |
| **E** | 000010000 |
| **F** | 000100000 |
| **G** | 001000000 |
| **H** | 010000000 |
| **I** | 100000000 |

Table 1: One-hot codes for the FSM.

Design and implement your circuit on your DE-series board as follows:

1. Create a new Quartus project for the FSM circuit.
2. Write a Verilog file that instantiates the nine flip-flops in the circuit and which specifies the logic expressions that drive the flip-flop input ports. Use only simple **assign** statements in your Verilog code to specify the logic feeding the flip-flops. Note that the one-hot code enables you to derive these expressions by inspection.

Use the toggle switch *SW*0 as an active-low synchronous reset input for the FSM, use *SW*1 as the *w* input, and the pushbutton *KEY*0 as the clock input which is applied manually. Use the red light *LEDR*9 as the output *z*, and assign the state flip-flop outputs to the red lights *LEDR*8 to *LEDR*0.

1. Include the Verilog file in your project, and assign the pins on the FPGA to connect to the switches and the LEDs.
2. Simulate the behavior of your circuit.
3. Once you are confident that the circuit works properly as a result of your simulation, download the circuit into the FPGA chip. Test the functionality of your design by applying the input sequences and observing the output LEDs. Make sure that the FSM properly transitions between states as displayed on the red LEDs, and that it produces the correct output values on *LEDR*9.
4. Finally, consider a modification of the one-hot code given in Table [1](#_bookmark41). It is often desirable to set all flip-flop outputs to the value 0 in the reset state.

Table [2](#_bookmark42) shows a modified one-hot state assignment in which the reset state, *A*, uses all 0s. This is accom- plished by inverting the state variable *y*0. Create a modified version of your Verilog code that implements this state assignment. (*Hint*: you should need to make very few changes to the logic expressions in your circuit to implement the modified state assignment.)

1. Compile your new circuit and test it.

|  |  |
| --- | --- |
| Name | State Code  *y*8*y*7*y*6*y*5*y*4*y*3*y*2*y*1*y*0 |
| **A** | 000000000 |
| **B** | 000000011 |
| **C** | 000000101 |
| **D** | 000001001 |
| **E** | 000010001 |
| **F** | 000100001 |
| **G** | 001000001 |
| **H** | 010000001 |
| **I** | 100000001 |

Table 2: Modified one-hot codes for the FSM.

## Part II

For this part you are to write another style of Verilog code for the FSM in Figure 2. In this version of the code you should not manually derive the logic expressions needed for each state flip-flop. Instead, describe the state table for the FSM by using a Verilog **case** statement in an **always** block, and use another **always** block to instantiate the state flip-flops. You can use a third **always** block or simple assignment statements to specify the output *z*. To implement the FSM, use four state flip-flops *y*3*, . . . , y*0 and binary codes, as shown in Table [3](#_bookmark43).

|  |  |
| --- | --- |
| Name | State Code  *y*3*y*2*y*1*y*0 |
| **A** | 0000 |
| **B** | 0001 |
| **C** | 0010 |
| **D** | 0011 |
| **E** | 0100 |
| **F** | 0101 |
| **G** | 0110 |
| **H** | 0111 |
| **I** | 1000 |

Table 3: Binary codes for the FSM.

A suggested skeleton of the Verilog code is given in Figure [3](#_bookmark44).

**module** part2 ( *. . .* );

*. . .* define input and output ports

*. . .* define signals

**reg** [3:0] y\_Q, Y\_D; // y\_Q represents current state, Y\_D represents next state

**parameter** A = 4’b0000, B = 4’b0001, C = 4’b0010, D = 4’b0011, E = 4’b0100, F = 4’b0101, G = 4’b0110, H = 4’b0111, I = 4’b1000;

**always** @(w, y\_Q)

**begin**: state\_table

**case** (y\_Q)

A: **if** (!w) Y\_D = B;

**else** Y\_D = F;

*. . .* remainder of state table

**default**: Y\_D = 4’bxxxx;

###### endcase

**end** // state\_table

**always** @(**posedge** Clock)

**begin**: state\_FFs

*. . .*

**end** // state\_FFS

*. . .* assignments for output z and the LEDs

###### endmodule

Figure 3: Skeleton Verilog code for the FSM.

Implement your circuit as follows.

1. Create a new project for the FSM.
2. Include in the project your Verilog file that uses the style of code in Figure 3. Use the same switches, pushbuttons, and lights that were used in Part I.
3. Before compiling your code it is necessary to explicitly tell the Synthesis tool in Quartus that you wish to have the finite state machine implemented using the state assignment specified in your Verilog code. If you do not explicitly give this setting to Quartus, the Synthesis tool will automatically use a state assignment of its own choosing, and it will ignore the state codes specified in your Verilog code. To make this setting, choose Assignments > Settings in Quartus, and click on the Compiler Settings item on the left side of the window, then click on the Advanced Settings (Synthesis) button. As indicated in Figure 4, change the parameter State Machine Processing to the setting User-Encoded.
4. Compile your project. To examine the circuit produced by Quartus open the RTL Viewer tool. Double-click on the box shown in the circuit that represents the finite state machine, and determine whether the state diagram that it shows properly corresponds to the one in Figure 2. To see the state codes used for your FSM, open the Compilation Report, select the Analysis and Synthesis section of the report, and click on State Machines.
5. Download the circuit into the FPGA chip and test its functionality.
6. In step 3 you instructed the Quartus Synthesis tool to use the state assignment given in your Verilog code. To see the result of removing this setting, open again the Quartus settings window by choosing Assign- ments > Settings, and click on the Compiler Settings item on the left side of the window, then click on the Advanced Settings (Synthesis) button. Change the setting for State Machine Processing from User-Encoded to One-Hot. Recompile the circuit and then open the report file, select the Analysis and Synthesis section of the report, and click on State Machines. Compare the state codes shown to those given in Table [2](#_bookmark42), and discuss any differences that you observe.

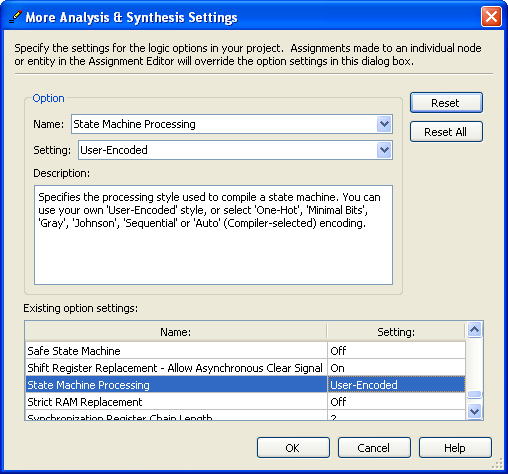


Figure 4: Specifying the state assignment method in Quartus.

## Part III

The sequence detector can be implemented in a straightforward manner using shift registers, instead of using the more formal approach described above. Create Verilog code that instantiates two 4-bit shift registers; one is for recognizing a sequence of four 0s, and the other for four 1s. Include the appropriate logic expressions in your design to produce the output *z*. Make a Quartus project for your design and implement the circuit on your DE- series board. Use the switches and LEDs on the board in a similar way as you did for Parts I and II and observe the behavior of your shift registers and the output *z*. Answer the following question: could you use just one 4-bit shift register, rather than two? Explain your answer.

## Part IV

In this part of the exercise you are to implement a Morse-code encoder using an FSM. The Morse code uses pat- terns of short and long pulses to represent a message. Each letter is represented as a sequence of dots (a short pulse), and dashes (a long pulse). For example, the first eight letters of the alphabet have the following represen- tation:

A • **—**

B **—** • • •

C **—** • **—** •

D **—** • •

E •

F • • **—** •

G **— —** •

H • • • •

Design and implement a Morse-code encoder circuit using an FSM. Your circuit should take as input one of the first eight letters of the alphabet and display the Morse code for it on a red LED. Use switches *SW*2−0 and pushbuttons *KEY*1−0 as inputs. When a user presses *KEY*1, the circuit should display the Morse code for a letter specified by *SW*2−0 (000 for A, 001 for B, etc.), using 0.5-second pulses to represent dots, and 1.5-second pulses to represent dashes. Pushbutton *KEY*0 should function as an asynchronous reset.

A high-level schematic diagram of a possible circuit for the Morse-code encoder is shown in Figure [5](#_bookmark45).

Pushbuttons and switches

LEDR0



Morse code length counter

Letter selection logic

Morse code shift register

FSM

Half-second counter

Data Enable Load

Data Enable Load

Figure 5: High-level schematic diagram of the circuit for Part IV.

PART 1

//KARTHIK J-1MS21EE028

module part1 (SW, KEY, LEDR);

input [1:0] SW;

input [0:0] KEY;

output [9:0] LEDR;

wire Clock, Resetn, w, z;

wire [8:0] y\_Q, Y\_D;

assign Clock = KEY[0];

assign Resetn = SW[0];

assign w = SW[1];

assign Y\_D[0] = 1'b0;

flipflop ff0(Y\_D[0], Clock, 1'b1, Resetn, y\_Q[0]);

assign Y\_D[1] = (y\_Q[0] | y\_Q[5] | y\_Q[6] | y\_Q[7] | y\_Q[8]) & ~w;

flipflop ff1(Y\_D[1], Clock, Resetn, 1'b1, y\_Q[1]);

assign Y\_D[2] = y\_Q[1] & ~w;

flipflop ff2(Y\_D[2], Clock, Resetn, 1'b1, y\_Q[2]);

assign Y\_D[3] = y\_Q[2] & ~w;

flipflop ff3(Y\_D[3], Clock, Resetn, 1'b1, y\_Q[3]);

assign Y\_D[4] = (y\_Q[3] | y\_Q[4]) & ~w;

flipflop ff4(Y\_D[4], Clock, Resetn, 1'b1, y\_Q[4]);

assign Y\_D[5] = (y\_Q[0] | y\_Q[1] | y\_Q[2] | y\_Q[3] | y\_Q[4]) & w;

flipflop ff5(Y\_D[5], Clock, Resetn, 1'b1, y\_Q[5]);

assign Y\_D[6] = y\_Q[5] & w;

flipflop ff6(Y\_D[6], Clock, Resetn, 1'b1, y\_Q[6]);

assign Y\_D[7] = y\_Q[6] & w;

flipflop ff7(Y\_D[7], Clock, Resetn, 1'b1, y\_Q[7]);

assign Y\_D[8] = (y\_Q[7] | y\_Q[8]) & w;

flipflop ff8(Y\_D[8], Clock, Resetn, 1'b1, y\_Q[8]);

assign z = y\_Q[4] | y\_Q[8];

assign LEDR[8:0] = y\_Q[8:0];

assign LEDR[9] = z;

endmodule

module flipflop (D, Clock, Resetn, Setn, Q);

input D, Clock, Resetn, Setn;

output reg Q;

always @(posedge Clock)

if (Resetn == 1'b0) // synchronous clear

Q <= 1'b0;

else if (Setn == 1'b0) // synchronous set

Q <= 1'b1;

else

Q <= D;

Endmodule

PART 2

//KARTHIK J-1MS21EE028

module part2 (SW, KEY, LEDR);

input [1:0] SW;

input [0:0] KEY;

output [9:0] LEDR;

wire Clock, Resetn, w, z;

reg [3:0] y\_Q, Y\_D;

assign Clock = KEY[0];

assign Resetn = SW[0];

assign w = SW[1];

parameter A = 4'b0000, B = 4'b0001, C = 4'b0010, D = 4'b0011, E = 4'b0100,

F = 4'b0101, G = 4'b0110, H = 4'b0111, I = 4'b1000;

always @(w, y\_Q)

begin: state\_table

case (y\_Q)

A: if (!w) Y\_D = B;

else Y\_D = F;

B: if (!w) Y\_D = C;

else Y\_D = F;

C: if (!w) Y\_D = D;

else Y\_D = F;

D: if (!w) Y\_D = E;

else Y\_D = F;

E: if (!w) Y\_D = E;

else Y\_D = F;

F: if (!w) Y\_D = B;

else Y\_D = G;

G: if (!w) Y\_D = B;

else Y\_D = H;

H: if (!w) Y\_D = B;

else Y\_D = I;

I: if (!w) Y\_D = B;

else Y\_D = I;

default: Y\_D = 4'bxxxx;

endcase

end // state\_table

always @(posedge Clock)

if (Resetn == 1'b0) // synchronous clear

y\_Q <= A;

else

y\_Q <= Y\_D;

assign z = ((y\_Q == E) | (y\_Q == I)) ? 1'b1 : 1'b0;

assign LEDR[3:0] = y\_Q;

assign LEDR[9] = z;

assign LEDR[8:4] = 5'b0;

endmodule

PART 3

//KARTHIK J-1MS21EE028

module part3 (SW, KEY, LEDR);

input [1:0] SW;

input [0:0] KEY;

output [9:0] LEDR;

wire Clock, Resetn, w, z;

reg [1:4] S4\_0s; // shift register for recognizing 4 0s

reg [1:4] S4\_1s; // shift register for recognizing 4 1s

assign Clock = KEY[0];

assign Resetn = SW[0];

assign w = SW[1];

always @(posedge Clock)

begin

if (Resetn == 1'b0)

begin

S4\_0s <= 4'b1111;

S4\_1s <= 4'b0000;

end

else

begin

S4\_0s[1] <= w;

S4\_0s[2] <= S4\_0s[1];

S4\_0s[3] <= S4\_0s[2];

S4\_0s[4] <= S4\_0s[3];

S4\_1s[1] <= w;

S4\_1s[2] <= S4\_1s[1];

S4\_1s[3] <= S4\_1s[2];

S4\_1s[4] <= S4\_1s[3];

end

end

assign z = ((S4\_0s == 4'b0000) | (S4\_1s == 4'b1111)) ? 1'b1 : 1'b0;

assign LEDR[3:0] = S4\_0s;

assign LEDR[7:4] = S4\_1s;

assign LEDR[9] = z;

assign LEDR[8] = 1'b0;

endmodule

PART-4

//KARTHIK J-1MS21EE028

module part4 (SW, CLOCK\_50, KEY, LEDR);

/\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*/

/\*\*\*\* PARAMETER DECLARATIONS \*\*\*\*/

/\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*/

// SW switch patterns, Morse codes, and code lengths are defined below (in the Morse

// code, 0 = dot, 1 = dash)

parameter A\_SW = 3'b000, A\_MORSE = 4'b0010, A\_LENGTH = 3'd2; /\* .- \*/

parameter B\_SW = 3'b001, B\_MORSE = 4'b0001, B\_LENGTH = 3'd4; /\* -... \*/

parameter C\_SW = 3'b010, C\_MORSE = 4'b0101, C\_LENGTH = 3'd4; /\* -.-. \*/

parameter D\_SW = 3'b011, D\_MORSE = 4'b0001, D\_LENGTH = 3'd3; /\* -.. \*/

parameter E\_SW = 3'b100, E\_MORSE = 4'b0000, E\_LENGTH = 3'd1; /\* . \*/

parameter F\_SW = 3'b101, F\_MORSE = 4'b0100, F\_LENGTH = 3'd4; /\* ..-. \*/

parameter G\_SW = 3'b110, G\_MORSE = 4'b0011, G\_LENGTH = 3'd3; /\* --. \*/

parameter H\_SW = 3'b111, H\_MORSE = 4'b0000, H\_LENGTH = 3'd4; /\* .... \*/

parameter s\_WAIT\_SEND = 3'b000, s\_WAIT\_BLANK = 3'b001, s\_SEND\_DOT = 3'b010,

s\_SEND\_DASH\_1 = 3'b011, s\_SEND\_DASH\_2 = 3'b100, s\_SEND\_DASH\_3 = 3'b101,

s\_RELEASE\_SEND = 3'b110;

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/\*\*\*\* PORT DECLARATIONS \*\*\*\*/

/\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*/

input [2:0] SW;

input [1:0] KEY;

input CLOCK\_50;

output [9:0] LEDR;

/\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*/

/\*\*\*\* LOCAL WIRE DECLARATIONS \*\*\*\*/

/\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*/

wire Clock, Resetn, go, half\_sec\_enable, load\_regs, shift\_and\_count, light\_on;

reg [3:0] morse\_code;

reg [2:0] morse\_length;

reg [3:0] send\_data;

reg [2:0] data\_size;

wire [1:0] pulse\_cycle;

reg [3:0] y\_Q, Y\_D;

/\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*/

/\*\*\*\* IMPLEMENTATION \*\*\*\*/

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assign Clock = CLOCK\_50;

assign Resetn = KEY[0];

assign go = ~KEY[1];

// FSM State Table

always @(go, y\_Q, send\_data, data\_size, half\_sec\_enable)

begin: state\_table

case (y\_Q)

s\_WAIT\_SEND:

if (go) Y\_D = s\_WAIT\_BLANK;

else Y\_D = s\_WAIT\_SEND;

s\_WAIT\_BLANK: // sync with the half-second pulses

if (!half\_sec\_enable)

Y\_D = s\_WAIT\_BLANK;

else if (send\_data[0] == 1'b0)

Y\_D = s\_SEND\_DOT;

else

Y\_D = s\_SEND\_DASH\_1;

s\_SEND\_DOT: // wait here for one half-second period

if (!half\_sec\_enable)

Y\_D = s\_SEND\_DOT;

else if (data\_size == 'd1) // check if we are done with this letter

Y\_D = s\_RELEASE\_SEND;

else

Y\_D = s\_WAIT\_BLANK;

s\_SEND\_DASH\_1: // wait for three half-second periods

if (!half\_sec\_enable)

Y\_D = s\_SEND\_DASH\_1;

else

Y\_D = s\_SEND\_DASH\_2;

s\_SEND\_DASH\_2: // wait for two more half-second periods

if (!half\_sec\_enable)

Y\_D = s\_SEND\_DASH\_2;

else

Y\_D = s\_SEND\_DASH\_3;

s\_SEND\_DASH\_3: // wait for one more half-second period

if (!half\_sec\_enable)

Y\_D = s\_SEND\_DASH\_3;

else if (data\_size == 'd1) // check if we are done with this letter

Y\_D = s\_RELEASE\_SEND;

else

Y\_D = s\_WAIT\_BLANK;

s\_RELEASE\_SEND:

if (~go) Y\_D = s\_WAIT\_SEND;

else Y\_D = s\_RELEASE\_SEND;

default: Y\_D = 3'bxxx;

endcase

end // state\_table

// FSM State flip-flops

always @(posedge Clock)

if (Resetn == 1'b0) // synchronous clear

y\_Q <= s\_WAIT\_SEND;

else

y\_Q <= Y\_D;

// FSM outputs

// turn on the Morse code light in the states below

assign light\_on = ( (y\_Q == s\_SEND\_DOT) | (y\_Q == s\_SEND\_DASH\_1) |

(y\_Q == s\_SEND\_DASH\_2) | (y\_Q == s\_SEND\_DASH\_3) );

// specify when to load the Morse code into the shift register, and length into the counter

assign load\_regs = (y\_Q == s\_WAIT\_SEND) & go;

// specify when to shift the Morse code bits and decrement the length counter

assign shift\_and\_count = ((y\_Q == s\_SEND\_DOT) | (y\_Q == s\_SEND\_DASH\_3)) & half\_sec\_enable;

/\* Create an enable signal that is asserted once every 0.5 of a second. \*/

modulo\_counter half\_sec( .Clock(CLOCK\_50), .Resetn(Resetn), .rollover(half\_sec\_enable) );

defparam half\_sec.n = 25;

defparam half\_sec.k = 25000000;

/\* Letter selection \*/

always @(\*)

case (SW)

A\_SW: begin morse\_code = A\_MORSE; morse\_length = A\_LENGTH; end

B\_SW: begin morse\_code = B\_MORSE; morse\_length = B\_LENGTH; end

C\_SW: begin morse\_code = C\_MORSE; morse\_length = C\_LENGTH; end

D\_SW: begin morse\_code = D\_MORSE; morse\_length = D\_LENGTH; end

E\_SW: begin morse\_code = E\_MORSE; morse\_length = E\_LENGTH; end

F\_SW: begin morse\_code = F\_MORSE; morse\_length = F\_LENGTH; end

G\_SW: begin morse\_code = G\_MORSE; morse\_length = G\_LENGTH; end

H\_SW: begin morse\_code = H\_MORSE; morse\_length = H\_LENGTH; end

endcase

/\* Store the Morse code to be sent in a shift register, and its length in a counter \*/

always@(posedge CLOCK\_50)

begin

if (~Resetn)

begin

send\_data <= 'd0;

data\_size <= 'd0;

end

else

if (load\_regs)

begin

send\_data <= morse\_code;

data\_size <= morse\_length;

end

else if (shift\_and\_count) // shift and decrement when appropriate

begin

send\_data[2:0] <= send\_data[3:1];

send\_data[3] <= 1'b0;

data\_size <= data\_size - 1'b1;

end

end

assign LEDR[0] = light\_on;

assign LEDR[9:1] = 9'b0;

endmodule

module modulo\_counter(Clock, Resetn, rollover);

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/\*\*\*\* PARAMETER DECLARATIONS \*\*\*\*/

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parameter n = 4;

parameter k = 16;

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/\*\*\*\* PORT DECLARATIONS \*\*\*\*/

/\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*/

input Clock, Resetn;

output rollover;

reg [n-1:0] Q;

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/\*\*\*\* IMPLEMENTATION \*\*\*\*/

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always@(posedge Clock)

begin

if (!Resetn)

Q <= 'd0;

else if (Q == k-1)

Q <= 'd0;

else

Q <= Q + 1'b1;

end

assign rollover = (Q == k-1);

endmodule